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5-Picosecond Photoconductive Sampling Oscilloscope

SBIR Phase I Final Report

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Steven Williamson

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ABSTRACT

During our Phase I SBIR we developed a novel laser-driven picosecond sampling photogate that has 5-picosecond temporal resolution and 10-micovolt sensitivity. The sampling gate system is evaluated and applied to several testing environments. To improve the sensitivity further, and lower the required excitation light level, we use a high-impedance transimpedance preamplifier stage. This amplifier permits us to measure signals down to 1 microvolt using less than 10 microwatts of average optical power. The sampling gate technology has now been extended to picosecond time-domain reflectometry measurements. Furthermore, we have coupled the picosecond sampling gate to a Picoprobe™ test probe to measure signals from circuits on wafer. This sampling gate system has now been applied by us to test all our high-speed photodetectors. Finally, we have engineered low-temperature MBE-grown $In_{0.25}Ga_{0.75}As$ (LT- $In_{0.25}Ga_{0.75}As$) that shows a temporal resolution of 4.2 picoseconds.

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A. Task Objectives

The primary objective of this Phase I program was to develop an impedance-matched sampling gate that has temporal resolution ≤ 5 picosecond (ps) and sensitivity of 100 microvolt (μV). The circuit that surrounds the sampling gate must preserve the frequency and phase content of the electrical signal as it is being sampled. To assure minimal reflections, the circuit (comprised of the launching electrodes, photogate and matching resistors) has submillimeter dimensions. We intended to develop the gate based on well-established low-temperature MBE-grown GaAs (LT-GaAs) and then move to LT- $In_{0.25}Ga_{0.75}As$ for long-wavelength applications. Unlike conventional GaAs, LT- GaAs is rich in arsenic traps to speed the response of the photogate. A 5-ps carrier lifetime was our target response.

B. Technical Problems

Sampling gate circuit development

To support sampling speeds as fast as 5 ps requires that we preserve the phase information over the full spectrum. This means addressing the problem of modal dispersion. The dielectric mismatch between the substrate (GaAs or InGaAs) and superstrate (air) is sufficiently large to create modal dispersion. This is especially true for transmission lines with transverse dimensions approaching 1 mm, as is required to mate to our coaxial geometry. The original approach that we proposed had us sampling the electrical signal as it moved down a transmission line. We found early on that the presence of the sampling gate significantly perturbed the electrical signal. We would need to design a sampling circuit that was properly impedance matched to the characteristic impedance of the transmission.

Another challenge before us was to develop a picosecond photogate with high sensitivity, or responsivity. For an MSM (metal-semiconductor-metal) finger spacing/width of 1 μm/1 μm, our previous results using LT-GaAs indicate that high sensitivity combined with picosecond

carrier lifetime is attainable. Though we anticipated even higher mobility from InGaAs, we designed and grew a more efficient structure to take full advantage of the MSM's nonuniform E-field profile.

Finally, no studies have been made of nonstoichiometric devices fabricated using direct-write e-beam lithography. We planned to use submicrometer e-beam lithography to reduce the finger spacing and width and improve the responsivity of the photogate.

InGaAs development

To develop the 5-ps InGaAs photoconductor, we first needed to eliminate the high leakage current encountered with nonstoichiometric LT-InGaAs. The high leakage current stems directly from low resistivity in the LT-InGaAs. Growing InGaAs at a temperature close to its polycrystalline temperature (160°C) creates an arsenic-rich epilayer. Upon annealing at the normal growth temperature of 550°C, these excess arsenic atoms coalesce into metal arsenic precipitates. To date, it is not clear whether it is the precipitates or the residual background concentration of excess arsenic that is responsible for reducing intrinsic carrier lifetime. Regardless of their respective roles, the lifetime of InGaAs can be reduced to less than 1 ps if grown at sufficiently low temperature. Although the excess arsenic is important for trapping the photogenerated carriers, it has the side effect of moving the Fermi level in InGaAs from midgap to near the conduction band. This decreases the material's resistivity.

We attempted early in our Phase I to compensate for the n-type effect that excess arsenic has on InGaAs by introducing a p-type dopant, namely beryllium. No improvement in resistivity was obtained. This perhaps is due to the low concentrations of Be tried (10^{17} cm^{-3} and 10^{18} cm^{-3}) compared to the level of excess arsenic we were incorporating (10^{20} cm^{-3}). Higher Be doping levels are attainable, however we risk introducing more defects which would further lower the material's resistivity.

C. General Methodology

Sampling gate design

Shown in Fig. 1 is the 50-Ω circuit geometry we designed for our sampling gate. Fine adjustments to the MSM photogate area, resistor strap, ground plane dimensions, and launching geometry were arrived at empirically through an iterative process using several design configurations. LT-GaAs was chosen as the test material for evaluating the various circuit designs. Its 1-ps carrier lifetime guarantees that any broadening in the output is due to the circuit.

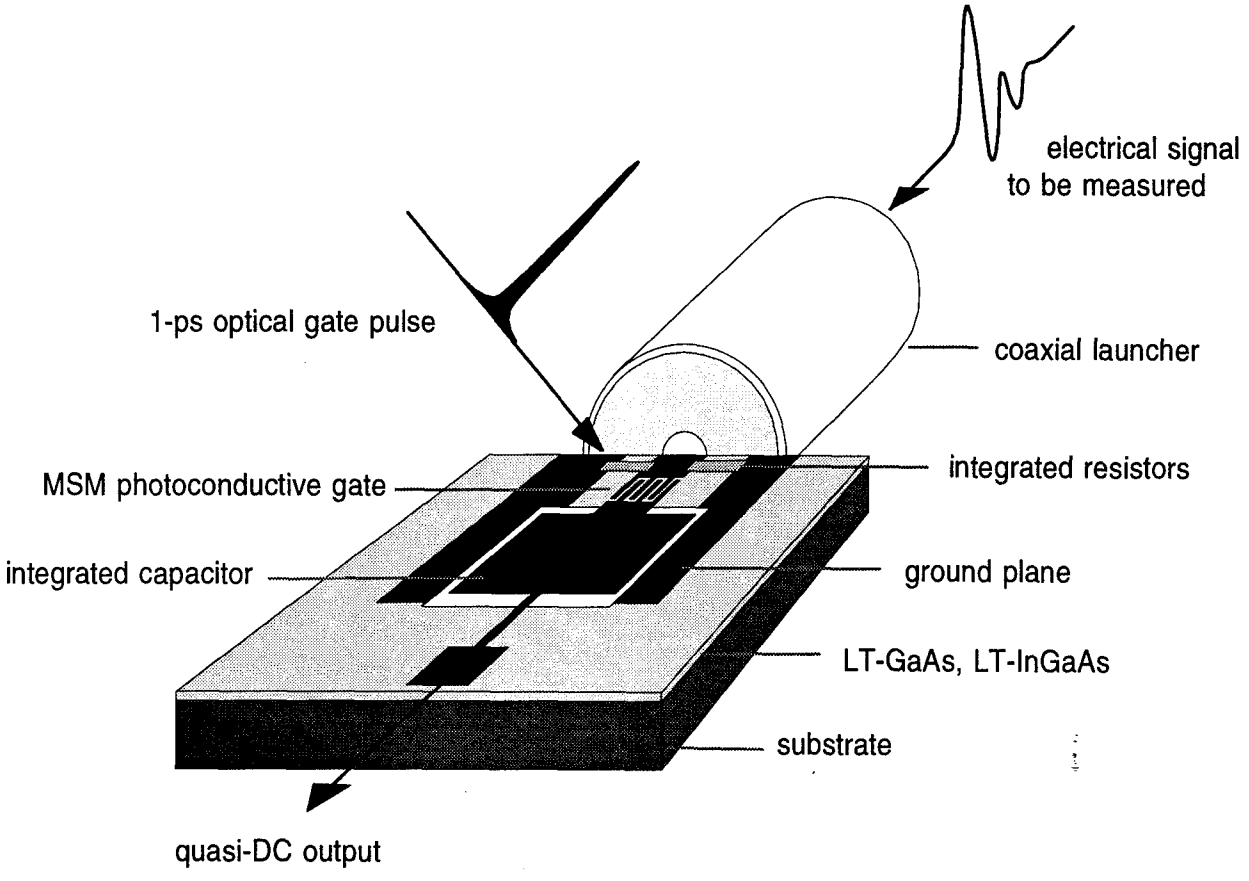


Fig. 1 Diagram of photogate circuit.

Sampling gate evaluation and applications

To test the photogate we used a mode-locked Ti:sapphire laser with < 100 fs pulse duration. We coupled our gate, using high speed 65-GHz rf connectors, to an equally fast (5 ps) pulse generator. The temporal response of the gate was measured along with its frequency response. We briefly studied saturation effects as the optical pulse level was increased.

With the sampling gate fabricated on LT-GaAs, we began testing in the traditional oscilloscope mode of operation. The sampling gate was also combined with a Picoprobe™ for on-wafer testing. The on-wafer probe measurements were of signals generated from a 5-ps photodetector. This detector is one of a matrix of detectors fabricated on a wafer. Each detector has its own 50-Ω termination and launching electrodes to mate to a 65-GHz Wiltron V-connector. The Picoprobe is dimensioned to emulate the launching environment found with the V-connector. An optical fiber delivery system is employed for both the detector and photogate.

We also demonstrated the application of the sampling gate for time-domain reflectometry (TDR). In the pure sampling gate mode of operation, the gate need only time-resolve the incoming electrical waveform. In the TDR mode of operation, two optical beams are incident on the MSM photogate. The first beam delivers a picosecond optical pulse (excitation pulse) that generates a ~5 ps electrical signal and is launched from the gate down the transmission line (or coaxial cable). As this electrical signal propagates down the transmission line it is subjected to discontinuities and other disturbances causing a fraction of the signal's energy to be reflected. The second beam delivers another 5-ps optical pulse (gate pulse) that is delayed relative to the excitation pulse and serves to sample the returning electrical signal. As with the Picoprobe, the TDR application is demonstrated using an optical fiber delivery system. This is most important, as the probe needs to be mobile and at the same time maintain picosecond temporal resolution.

MBE growth of InGaAs

We conducted our InGaAs materials studies using $In_{0.25}Ga_{0.75}As$ grown on GaAs as the active layer rather than going straight to lattice-matched $In_{0.53}Ga_{0.47}As$ grown on InP. We learned from previous work that the resistivity of LT-$In_xGa_{1-x}As$ drops exponentially with indium concentration. A value x = 0.25 places us midway between GaAs (where LT-GaAs has a demonstrated resistivity $>10^7\Omega$-cm) and $In_{0.53}Ga_{0.47}As$. During the Phase I we restricted our effort to testing the *speed* of LT-$In_{0.25}Ga_{0.75}As$. The development of LT- $In_{0.25}Ga_{0.75}As$ with *high resistivity* will also be essential before this material can be properly utilized in a sampling gate. This area of research will be taken up during our Phase II.

To make the transition from the GaAs substrate to $In_{0.25}Ga_{0.75}As$ we grew a graded layer that increased in In concentration from 0-25%. Figure 2 shows a cross sectional view of this structure. The photogate was designed for light incident from the top surface, between the electrodes. To maximize sensitivity, we placed high-sensitivity, stoichiometric InGaAs near the surface where the light is predominately absorbed and where the E-field strength between the electrodes is strongest. By adjusting the thickness of the $In_{0.25}Ga_{0.75}As$ top layer, we can change the photogate's sensitivity at the expense of speed or *vice versa*. Three structure with $In_{0.25}Ga_{0.75}As$ thickness 1600Å, 2200Å, and 2700Å were tried.

The electric field lines formed when a bias is applied are also drawn in Fig. 2. These field lines are typical of field patterns in MSM structures, as modeled using 1-dimensional simulations.[1] We see that the field is greatly enhanced at the anode, giving rise to hole (minority) current orders of magnitude larger than the electron (majority) current. With a voltage applied, the depletion width of the reverse biased contact increases, while the depletion width of the forward bias contact decreases. Holes generated sufficiently deep in the active region actually sink further in the presence of the strong field at the anode. To assure that holes lost to the substrate will not return to form a long response tail, we grew the LT-$In_{0.25}Ga_{0.75}As$ layer with a thickness of 2000 Å. The probability of carriers (electrons or holes) moving across a 2000-Å thickness of trap-rich LT-$In_{0.25}Ga_{0.75}As$ layer is very low.

InGaAs testing

The MSM photogates were first DC-tested for leakage current, hold-off voltage, and responsivity. To assure the lowest possible leakage current, we etched away the $In_{0.25}Ga_{0.75}As$ heterostructure everywhere except where the photogate was to be fabricated. This forms a mesa on which we fabricated our MSM photogates.

We measured the speed of the LT-InGaAs material using the technique of picosecond photoconductive sampling.[2] As with the more common technique of electro-optic sampling [3], photoconductive sampling is a pump-probe measurement. In addition to having higher sensitivity and less ambiguity, photoconductive sampling makes a direct voltage measurement rather than reading the electric field. Our photoconductive probe is not integrated in the device under test, but is free-standing and noninvasive with a temporal resolution less than 2 ps. High-speed coplanar stripline structures were fabricated on the LT-InGaAs with the MSM photogates bridging the electrodes.

Figure 3 shows a photomicrograph of the integrated MSM photogate-coplanar stripline on InGaAs. As with the DC devices, we etched through to the substrate, except where the photogate is fabricated. The mesa for the stripline is formed as a strip mesa oriented perpendicular to the transmission lines and across the intended photogate region. We etched away the excess InGaAs for the speed measurements to reduce high-frequency losses associated with the coupling of the electric field in the low-resitivity substrate. We also deposited a 2000-Å layer of SiO_2 on the now-exposed InP surface before depositing the coplanar electrodes. All measurements were made using a mode-locked Ti:Sapphire laser with a pulse duration of 0.1 ps. The center wavelength for the laser is 800 nm.

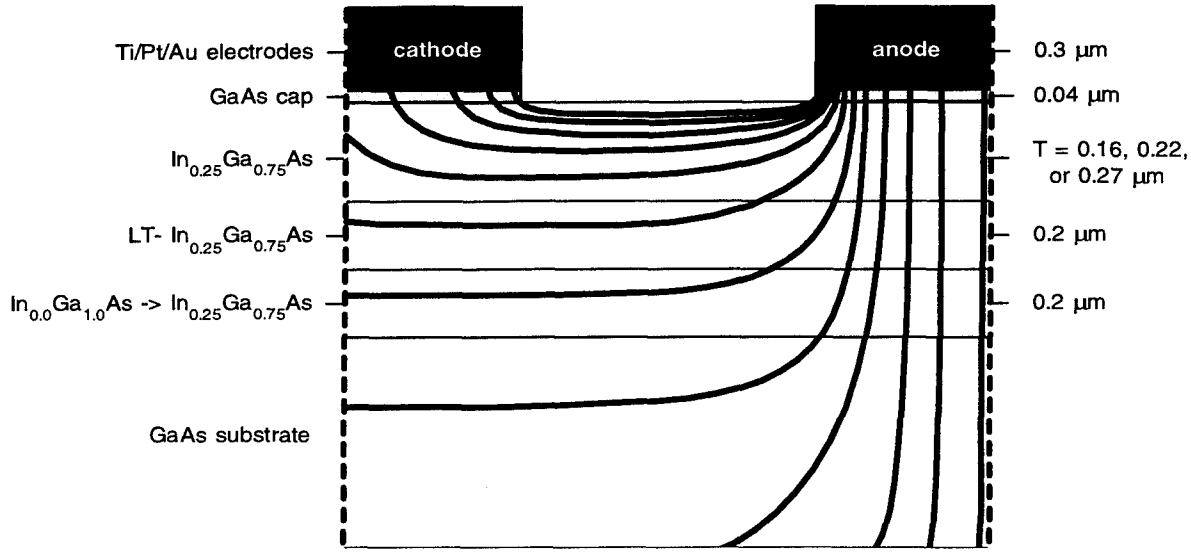


Fig. 2 Profile of LT-$In_{0.25}Ga_{0.75}As$ epitaxial heterostructure grown on GaAs. The dark lines show the path of the electric field with a bias voltage applied.

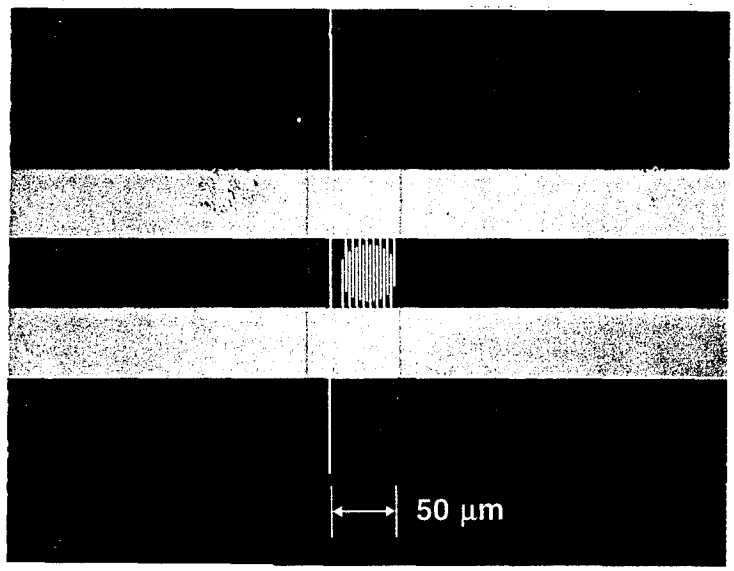


Fig. 3 Transmission line structure for characterizing the carrier lifetime of LT- $In_{0.25}Ga_{0.75}As$.

D. Technical Results

Photogate development

Figure 4 shows a photomicrograph of the picosecond photogate depicted in Fig. 1. The MSM photogate has a diameter of 50 μm to match to 50-μm core graded index multimode fiber. The signal to be measured leaves the coaxial environment and charges the sampling photogate with a time-varying 'bias'. The gate signal closes the photogate for 1 ps causing the current present at that moment to pass. The matched terminating resistors greatly reduce reflections and variations to the frequency response. The completed photogate structure requires seven mask levels to fabricate. The connectors used are Wiltron™ V-type connectors and are designed to operate up to 65-GHz. We keep the length of the transmission line as short as possible to reduce modal dispersion. Even with its length of 100 μm, modal dispersion can be problematic if the spacing between the ground line and the center line is large. In our structure this spacing is

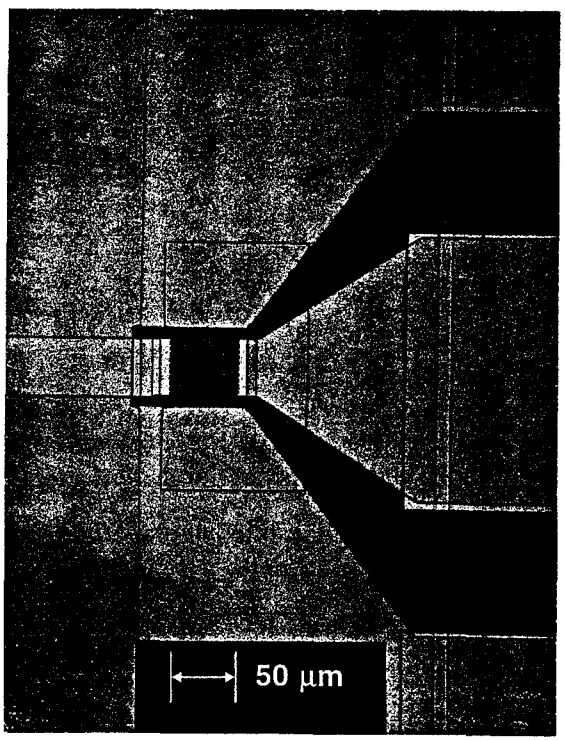


Fig. 4 Photomicrograph of picosecond LT-GaAs MSM photogate.

100μm, determined by the coaxial launcher dimensions. The dielectric constant used in the coaxial launcher is 3, allowing transverse dimensions up to ~ 1mm to be used without exciting higher order modes. With GaAs or InGaAs, the dielectric constant is 13. With air as the superstrate medium, the effective dielectric drops to ~ 7. Previous measurements made in our lab using similarly dimensioned transmission lines on GaAs have shown that pulse broadening after 500 μm of travel amounts to less than 2 ps. In Fig. 5 we see a magnified view of an MSM photogate. The interdigitated fingers were designed on the mask to have a 1.5 μm separation and 1.0 μm width. Instead, we measure fingers that have a 1.2 μm separation and 1.3 μm width. This change in the finger dimensions is caused by over processing the photoresist prior to depositing the gold. Along with a reduction in sensitivity, we also observe a slowing of the

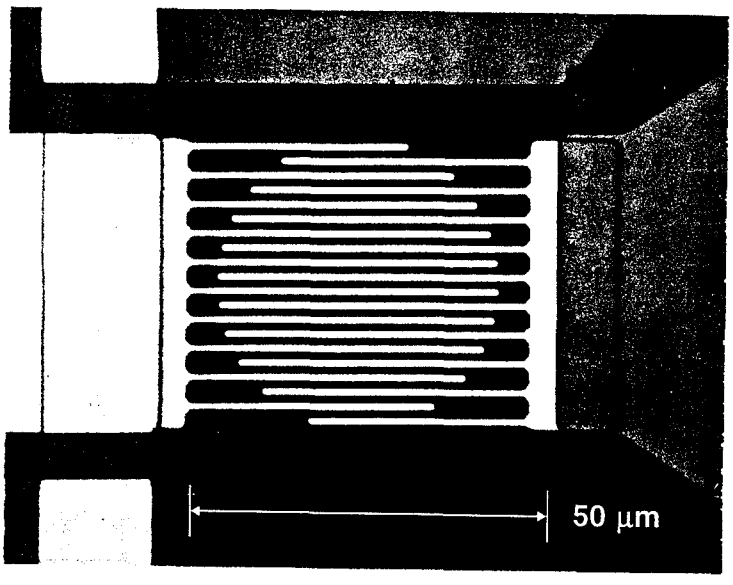


Fig. 5 Magnified view of the MSM interdigitated fingers.

response due to an increase in capacitance. When the photoresist process is optimized we find that the interdigiated fingers match to the mask to within 5% error.Figure 6 shows an equivalent circuit for the photogate. Given the dimensions of the elements comprising the circuit, we can model this as a lumped element, even at 65 GHz. Figure 7 shows the performance of the MSM photogate circuit using LT-GaAs. We see that the waveform is quite symmetric about its peak, which indicates that the circuit combined with the coaxial launcher shows little dispersion. The response time (measured as the full-width-at-half-maximum) is 7 ps. With the sampling gate's response unfolded, this reduces to 5 ps. The -3-dB roll off for this device is 60 GHz. This is very encouraging. We are now limited by the rf-connectors.

A unique aspect of this photogate technology is that we can develop our own picosecond diagnostic techniques, the most significant of which is a time-domain-reflectometer (TDR) for picosecond electrical pulses. TDR's have traditionally been of great utility in both electrical and optical fields. However, they have never been successfully been employed in the picosecond domain due to an absence of technology at this temporal level. Preliminary TDR experiments have already demonstrated this capability and a proposed "dual-gate" TDR structure is shown in Fig. 8. The drawing shows two gates connected in parallel. The first has a DC bias applied and operates as a pulse generator which launches a pulse into the structure to be tested. The second gate operates as a photogate and samples the reflected waveform with picosecond resolution. In this experiment, a 10 picosecond pulse was launched into a short length of coaxial cable, shorted at the opposite end. Both the launched signal and the return are measured by the photogate. The result of the TDR mode of operation is shown in Fig. 9. We clearly see the expected inverted pulse returning 230 ps later, but its broadening is also indicative of the dispersion encountered along the line.

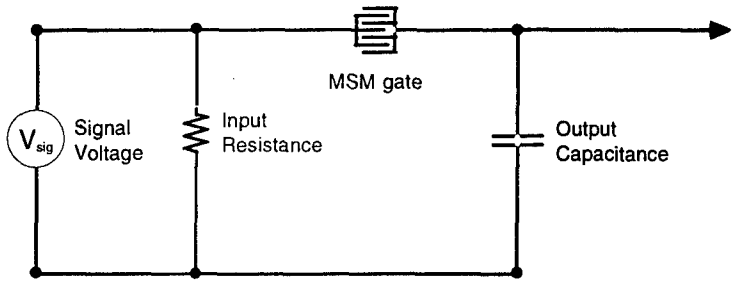


Fig. 6 Equivalent circuit for photogate.

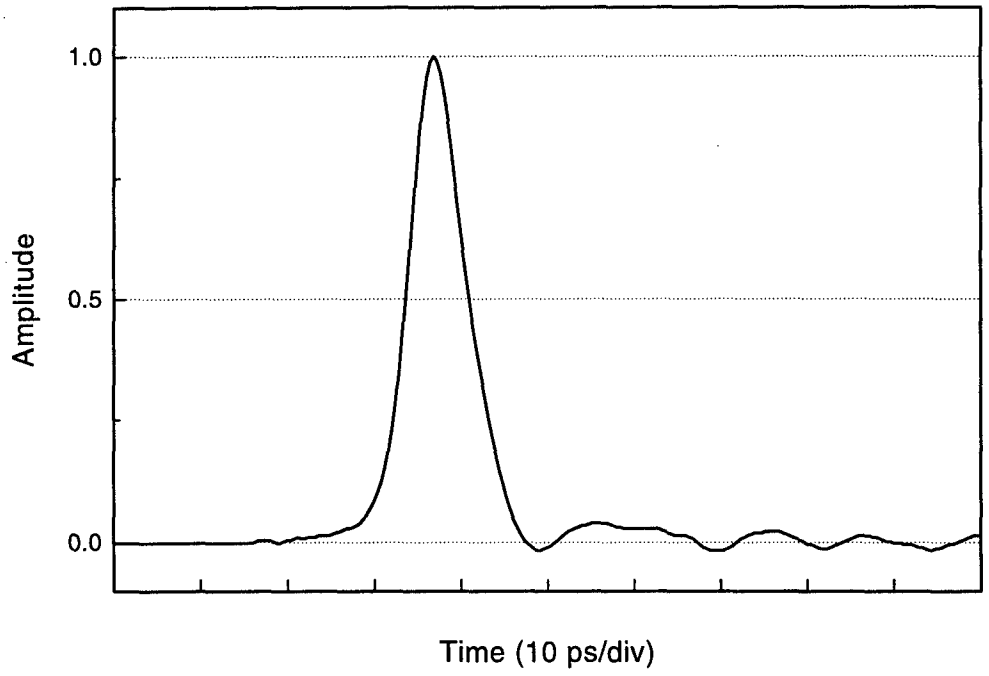


Fig. 7 Temporal response of the picosecond LT-GaAs MSM photogate.

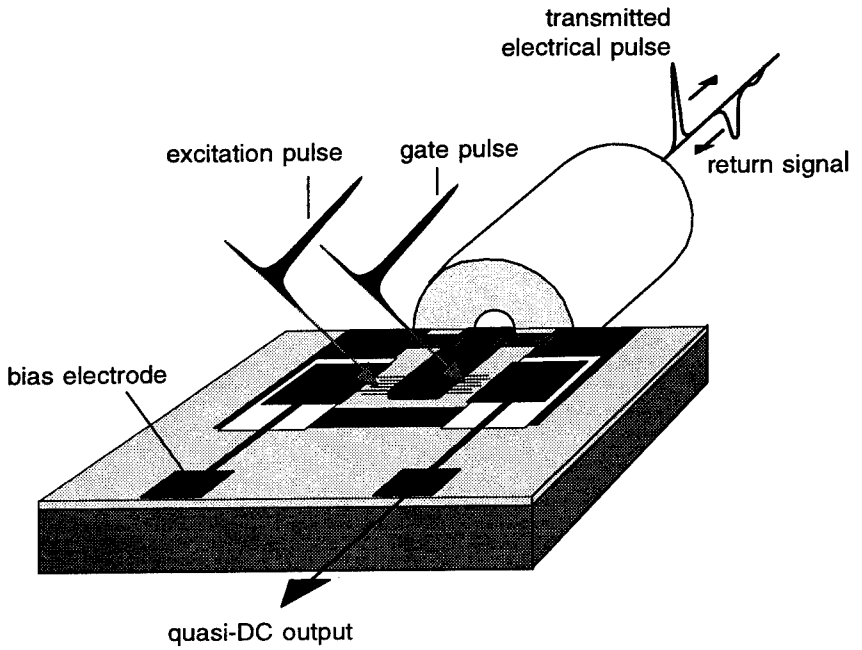
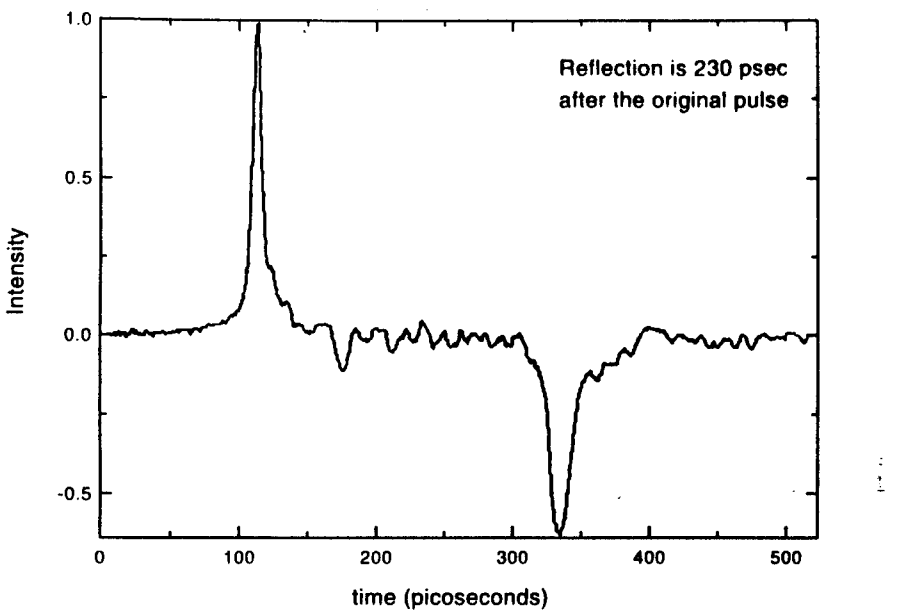


Fig. 8 Picosecond sampling time-domain reflectometer (TDR) using the photoconductive sampling gate.



Fig, 9 Using the photogate in TDR mode. The result of generating a picosecond electrical pulse and time-resolving both the launched and reflected signals.

Direct-write e-beam lithography

During our study of arsenic-rich non-stoichiometric semiconductors we fabricated MSM photogates using direct e-beam lithography. Direct e-beam fabrication offers us a straight forward means to produce submicrometer lithography. We have discovered a potential problem when we use e-beam lithography with non-stoichiometric materials. The primary electron beam has an energy of 40 KeV, which is sufficiently energetic to penetrate through the photoresist and into the semiconductor. These electrons come to rest 1-2 μm into the semiconductor after losing energy, mostly by interacting with weakly bond electrons. Studies exist that link the use of e-beam lithography to reduced device performance. However, the reduction in performance is usually quite small and more than off set by the many benefits of using direct write e-beam.

It now appears that non-stoichiometric semiconductors could be an exception. With non-stoichiometric GaAs, we do observe a marked reduction in responsivity when we fabricate using direct-write e-beam lithography. Figure 10 shows data taken of two samples, each fabricated with optical and e-beam lithography. One sample is conventionally-grown GaAs using MOCVD. The other sample is nonstoichiometric GaAs grown at 300°C using MBE. On each sample we fabricated MSM photogates using direct e-beam and optical lithography with equal finger spacings and widths of 1.5 μm. The photogates are illuminated with 100 μW of light at λ=633 nm over the entire 50x50 μm^2 area. For the stoichiometric sample, the relative sensitivity of the optical and e-beam lithography techniques differ by at most a factor of two. This discrepancy can be caused by unequal finger width/spacing that result from overprocessing the photoresist. Ideally, the relative sensitivity for the two techniques should be the same. For the non-stoichiometric GaAs samples, the sensitivity for both fabrication techniques are lower than their stoichiometric counterparts, with the e-beam-written photogate being considerably lower. Finally, we see that the sensitivity of the non-stoichiometric photogate fabricated using e-beam decays over time. The dramatic drop in sensitivity must be caused by the direct-write e-beam process. The reason is still unclear. Regardless, a technique for preventing these energetic electrons from entering the LT-region will need to be developed before direct-write e-beam lithography can be used. Until this time, (sub)micrometer optical lithography will have to do.

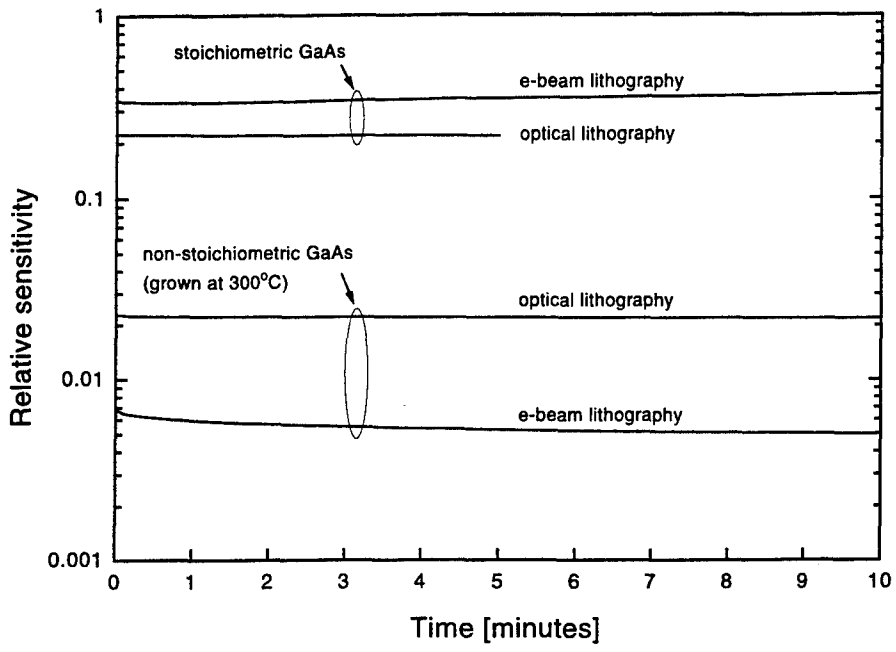


Fig. 10 Sensitivity of stoichiometric and nonstoichiometric photogates fabricated with optical and direct-write e-beam lithography.

Post-amplification of the photogate

One problem with the photogate is that it disturbs the signal being measured by draining away excessive current. This signal also tends to be weak in amplitude at the oscilloscope input, yielding a poor signal-to-noise. Problems are further exacerbated by the large output capacitance encountered with the coaxial cable used to deliver our signal to the oscilloscope. At 25 pF/foot, the gate must deliver a large amount of charge in order to obtain a reasonable voltage signal. Furthermore, since the measured voltage of our gate depends on the length of our output cable, we are not able to properly measure the true voltage on our device under test (DUT).

In order to help transform our gate into a noninvasive measuring device and also be able to get an absolute voltage measurement we must change our gate from a *current*-monitor into a

voltage-monitor. This can be accomplished by using a JFET-source follower which acts as both a buffer between our gate and oscilloscope and as a power amplifier to help drive the oscilloscope input. This is done by providing a lower capacitance and a higher resistance at the gate output in order to allow measurements to be made by drawing much less current and charge. Figure 11 shows the source follower used as our transimpedance amplifier (TIA). The top JFET, Q1, acts as the actual source follower with the output source voltage following the input gate voltage. The other JFET, Q2, acts as a current source draining just enough current so that $V_{GS}=0$ and fixing our offset to zero volts. This circuit design is fairly common and was chosen for a couple of reasons. First of all, the input capacitance of the JFET can be made very small (the newest design has $C_{input}=1.7$ pF), thus allowing us to measure voltages by sampling very small amounts of charge. Secondly, the small leakage current, I_{GS} (typically 1 pA), of the JFET clamps our gates leakage current at this level, thus allowing us more freedom to choose material being used for the gate. Finally, we can achieve accurate voltage readings of our DUT with quite modest light levels on our gate.

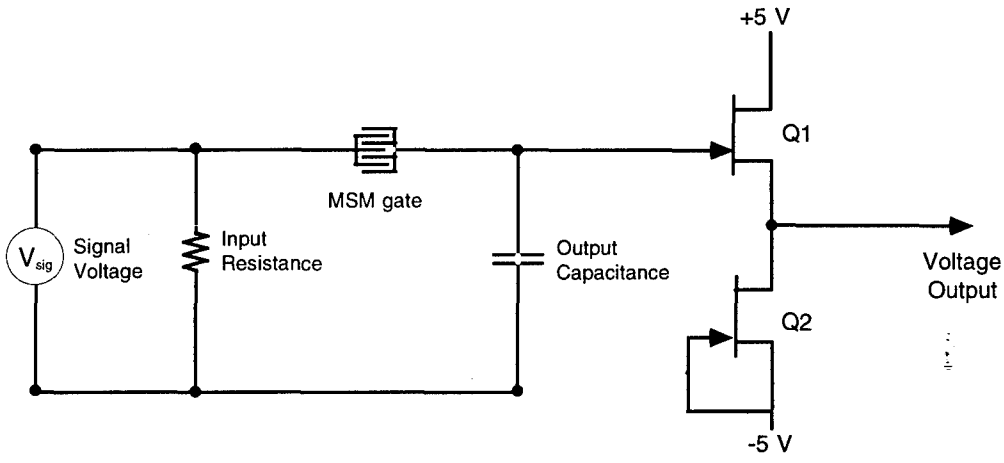


Fig. 11 Circuit diagram of the picosecond sampling gate with source follower.

For the TIA that was used in our experiment we had an output capacitance of 12 pF and leakage current of 1 pA. The matched pair of JFET's was supplied using a 2N5512 transistor pair that were directly wired to the output of our gate and all contained in a gold module in order to shield from any external noise source. In order to determine how the amplifier performed, two sets of data were taken. The first measurement was taken using a typical Picometrix, PX-D14 detector being sampled by a 4.5-ps, MSM gate without a post-amplifier. The second set of data was taken by using the same detector input with a 4.5-ps, MSM gate followed by a TIA. In each case data was taken with 300 μW of light input into the PX-D14. The results, shown in Figure 12, illustrate the advantage of the TIA. An improvement of up to 150 in output voltage is gained at an input light level of 200 nW. More importantly, the output voltage saturates when the TIA is

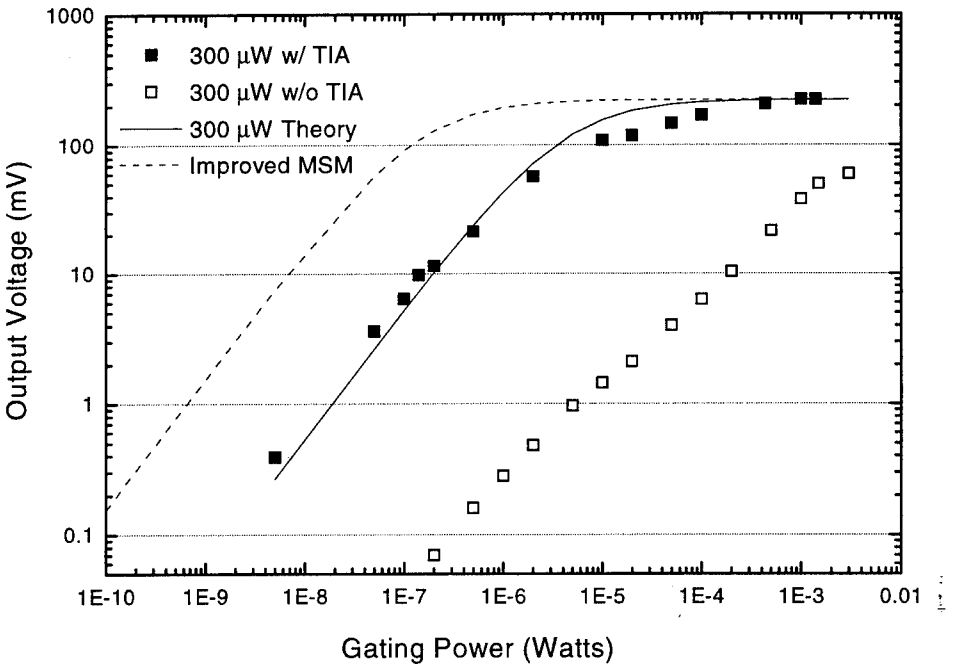


Fig. 12 A voltage signal with a peak of 222 mV is applied to the gate with (dark squares) and without (open squares) a transimpedance amplifier. Modeling is done to match the experiment(solid line) and show the performance of an improved design (dashed line).

used. The decreased output capacitance allows the sampled voltage to follow that of the signal accurately, even when the gate's on-state resistance is relatively large. This means that by using a large light level (1 mW) on the gate the output voltage is immune to fluctuations in the laser-gating power. This also allows one to get a true measure of the voltage on our DUT, in our case that corresponds to 222 mV. Another option is to use only enough power to switch 50% of the voltage signal. For our case this corresponds to only 10 μW of gate power. By applying different voltage levels it found that this is always the 50% switching power, as expected. At this modest level, almost any optical source can be used, thus freeing up the optical power for switching the DUT or other needs.

Changing our current-sampling gate into a voltage-sampling circuit with a high input impedance, permits us to develop a non-invasive, absolute voltage measurement system. The sensitivity is high, able to detect voltages down to 100 μV, and, as mentioned, the laser power required for accurate voltage measurements can be as low as 10 μW, even lower for larger signals or non-absolute measurements. The behavior of the gate with a source follower is seen to have basically two operating regimes. One is a low-gate power, linear regime, and the other is the saturation region. By employing a basic charge-injection/dissipation model for the system we can explain this two-regime nature of the amplifier. With a high repetition rate laser (100 MHz) and a low average power, we can approximate our output voltage by

$$V_{out} = \frac{\eta PR}{1+\eta PR} V_{signal}$$

where η is the gate responsivity per voltage applied, P is the average optical power, and R is the dark resistance of the gate. For our gate η=(0.008 A/W)/(5 Volts)=0.0016 A/W-V and R=150 MΩ. By using our saturated measured voltages as V_{signal} we have plotted the calculated V_{out} in Figure 2. As can be seen, there is some discrepancy between the theory and experiment. The data sags in the saturation region of the plot and does not reach saturation as quickly as expected. We believe this is due to using our current source, Q2, at I_{DSS}, where it does not behave as a

really good current source as needed. If we add a matched pair of resistors to the source of each JFET we can use a lower current source value and improve the saturation behavior of our device.

Other improvements in the present design could be implemented. At present, the two JFET's are not perfectly matched and a DC-offset of about 30 mV is present. It is hoped that by using a better matched pair of JFET's the DC-offset will be reduced. Adding the two resistors could also contribute to the offset if they are not matched, so they too, will have to be well balanced.

In order to lower the laser power necessary to reach saturation we must either increase the dark resistance of our gate or increase the responsivity. Since we are working with a gate we have good control of our light source and we could envision shrinking down the area of our MSM by a factor of 25 which would give us a corresponding drop in the dark resistance. Due to the nature of photoconductive material, we would not want to increase the material responsivity since this usually comes at the expense of speed; therefore, we must look to increase the available surface area open to light in the MSM's. This could be done by using a larger spacing-to-finger-size ratio. At present we have 1.5 μm spacing with 1 μm fingers. By going to 0.5 μm fingers while retaining the spacing we can expect a 15% increase in responsivity. The improved performance is shown as the dashed line in Fig. 12. As can be seen, with this new design we should be able to get an absolute voltage measurement with only 1 μW of gate light. While increasing our dark resistance we must also decrease our output capacitance in order to retain our sampling bandwidth, otherwise the rate at which we can collect data will be compromised. At present, there are transimpedance amplifiers with input capacitance's of less than 100 fF which would offset the rise in dark resistance thus allowing us to retain our sampling bandwidth.

In conclusion, the use of a post-amplifier after our gate has allowed us to convert our current-sampling gate into a voltage-sampling gate thus reducing the invasiveness of our oscilloscope. The amount of light required to fully switch the measured voltage was found to be around 100 μW and levels as low as 100 nW give us usable output signals. By making improvements in the amplifier design, full switching should be attainable with light levels on the order of 1 μW.

Using a on-wafer probe with the photgate

When testing an array of on wafer microwave devices before assembly or when testing a certain location on a complicated microwave circuit there is a need for on-wafer measurements that can be done with minimal invasion of the circuit. A probe is needed to reach down and contact the circuit, taking the signal to a conveniently located measurement device.
The Picoprobe is one type of wafer probe, and it is uniquely suited to work with our 5-ps gate/amplifier. By housing both our optical gate and the JFET source follower in a gold module, the entire unit can be mounted directly onto the back of a Picoprobe as shown in Fig. 13.

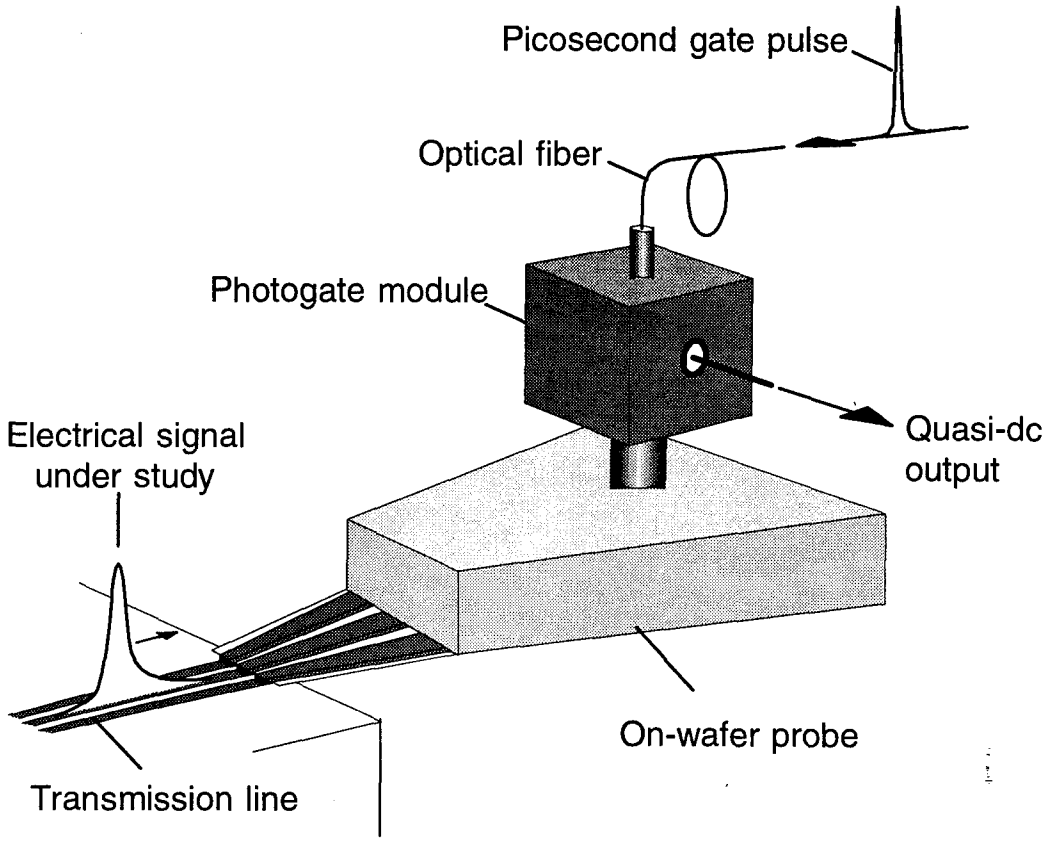


Fig. 13 Amplified picosecond photogate in use with on-wafer probe

The optical gating pulse is then fiber delivered to the gate and the quasi-DC output can be taken by displayed by a slow-oscilloscope. In the example shown in Fig. 13 we see an electric signal propagating on a transmission line and being launched onto the on-wafer probe. Although shown as being at the end of the wafer, the low-profile of this probe allows us to test a transmission line at any point in a circuit and at any location on a wafer. Furthermore, the probe could be used in conjunction with a biased MSM gate to act as a picosecond-electrical pulse generator. Thus, more complicated testing of a microwave circuit could be done by using two probes in concert.

We have tested this device with our gate/amplifier combination to measure a 4-by-6 array of photodetectors on wafer. By doing this we are able to quickly determine performance of an entire fabrication run rather than having to fully assemble a detector module in order to test just one representative device. The more complete and more rapid testing gives us the ability to improve our fabrication techniques in order to get uniform performance from our detectors. The test result is shown in Figure 14.

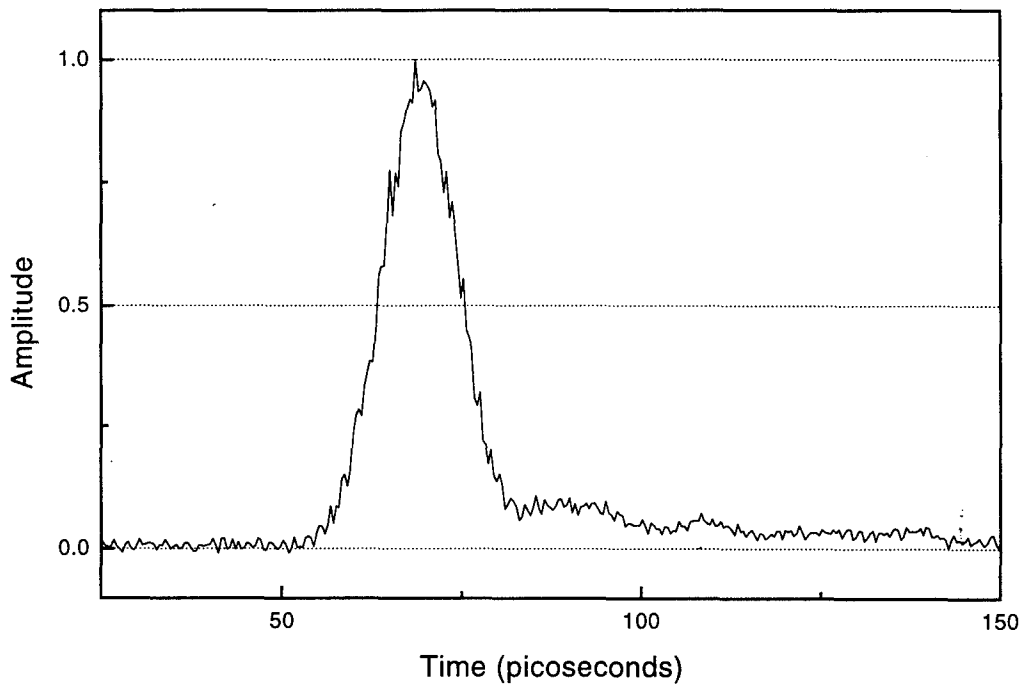


Fig. 14 Result on using photogate with an on-wafer probe to test wafer-level photodetectors.

A comparison with the fully assembled detector would show almost no change in the impulse response of the detector thus showing the quality of the on-wafer testing. The Picoprobe/gate combination has a bandwidth of 65 GHz limited by the Wiltron-V connector used to connect the probe and the gate/amplifier module. The system is minimally invasive to the device under test, as discussed in the previous section, since it leaks off only picoamps of current. Due to the design of the Picoprobe, it can work for more than 25 million trials, making it a very rugged and reliable way to do on-wafer testing.

$In_{0.25}Ga_{0.75}As$ development

It is challenging to grow epitaxial $In_{0.25}Ga_{0.75}As$ films on GaAs that are free of cross hatch and oval defects. This is especially true when growing films at temperatures as low as 160°C. We grow our structures as near to this temperature as possible to maximize excess arsenic.

Our first attempt at growing the heterostructure was unsuccessful. Figure 15 shows a Nomarski photomicrograph of its surface. The orthogonal relief is evidence of cross hatch, while the small white spots are oval defects. Photogates made of this material were found to have leakage currents exceeding 10mA, several orders of magnitude higher than that obtained with conventional $In_{0.53}Ga_{0.47}As$ lattice-matched to InP. We reduced the thickness of the buffer layer and decreased the periodicity of the digital superlattice that forms the graded region. These changes eliminated the cross hatch and significantly reduced the oval defect density.

Preliminary studies showed the leakage current to be less than 1 nA. Once this was under control we grew three heterostructures with $In_{0.25}Ga_{0.75}As$ layer thickness of 1600Å, 2200Å, and 2700Å, grown directly on a 2000-Å thickness of LT-$In_{0.25}Ga_{0.75}As$. The purpose of growing the three thicknesses was to determine the importance of excess arsenic in InGaAs, as it relates to the carrier lifetime. The leakage current for these structures, with 50-μm diameter photogates having 2-μm finger spacing/widths and biased to 5 volts, was less than 50 nA. Photogate/transmission line structures were then fabricated on these heterostructures. The symmetric nature of the MSM structure allows either electrode of the transmission line to be biased to 5 volts with the adjacent

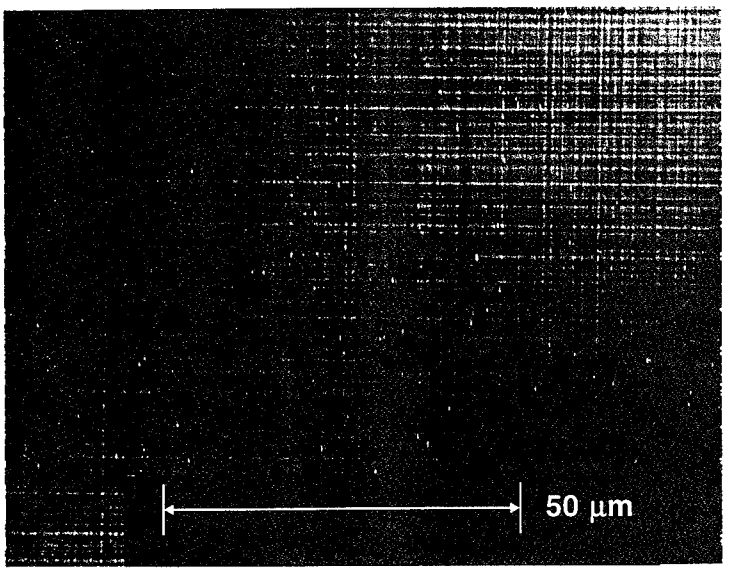


Fig. 15 Nomarski photograph of the surface of an LT- $In_{0.25}Ga_{0.75}As$ sample grown on GaAs. Poor crystal quality in this sample is evidenced by the cross hatching.

line tied to ground. We placed the photoconductive sampling probe on the ground electrode. Light incident on the photogate causes charge to transfer to the ground electrode. This forms the displacement current pulse that propagates down the line and is measured by the picosecond probe. As this current pulse moves down the transmission line, it is time-gated by our sampling probe. For these measurements, we probed the electrical signal 50 μm from the photogate. The transmission line is capable of supporting pulses as short as 1 ps over a propagation distance of 1 mm.

Figure 16 shows the temporal response for $In_{0.25}Ga_{0.75}As$/LT- $In_{0.25}Ga_{0.75}As$ photoconductor with a $In_{0.25}Ga_{0.75}As$ thickness of 1600 Å. The response time is 4.2 ps. After unfolding the probe's response (~ 2 ps), the photoconductor's own response is 3.7 ps. For an active area of 50x50 μm^2, this is the fastest LT-$In_{0.25}Ga_{0.75}As$ photoconductor demonstrated to

date. The second peak on the shoulder is a reflection from the sampling gate of the probe. The frequency response for this sample is shown in Fig. 17. Here, we see the -3 dB point is 60 GHz, taken *before* the probe's response is unfolded. We note that this photogate has a usable frequency content out to 150 GHz.

The sample used for these measurements is the thinnest of the three $In_{0.25}Ga_{0.75}As$ layers grown, with a responsivity of only 0.1 A/W. We are currently using 2-μm finger widths and spacing for the MSM electrodes. As we reduce these dimensions to 1 μm or less, we will see sensitivity continue to rise. A smaller electrode spacing means the carriers will travel a greater fraction of the distance between electrodes before being trapped. This increase in the fractional excursion translates directly into a net increase in photocurrent.

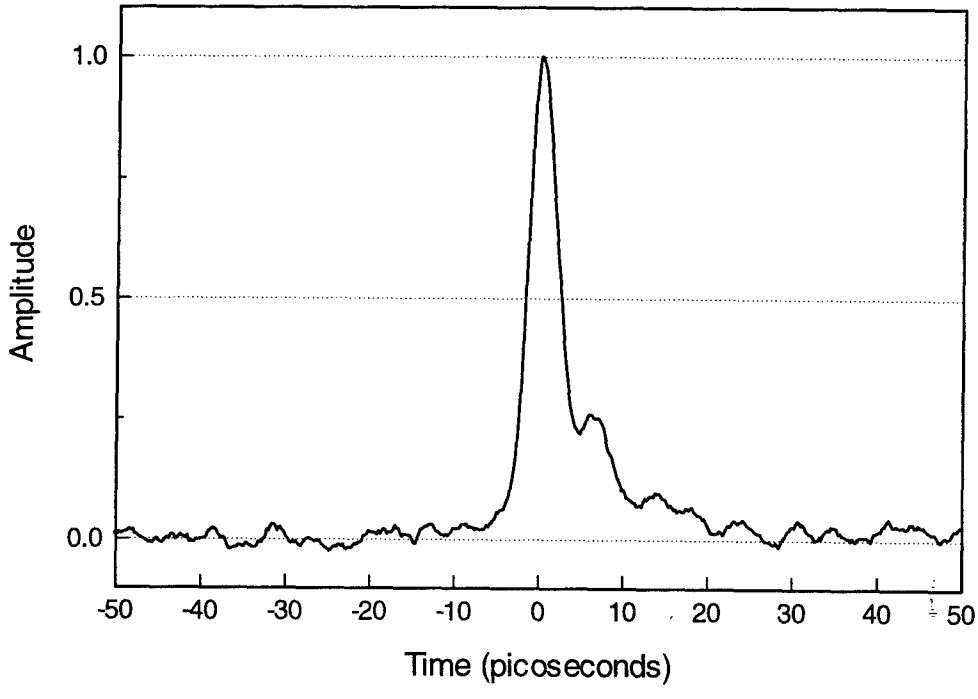


Fig. 16 Temporal response of LT-$In_{0.25}Ga_{0.75}As$ / $In_{0.25}Ga_{0.75}As$ photoconductor for an $In_{0.25}Ga_{0.75}As$ thickness of 1600 Å.

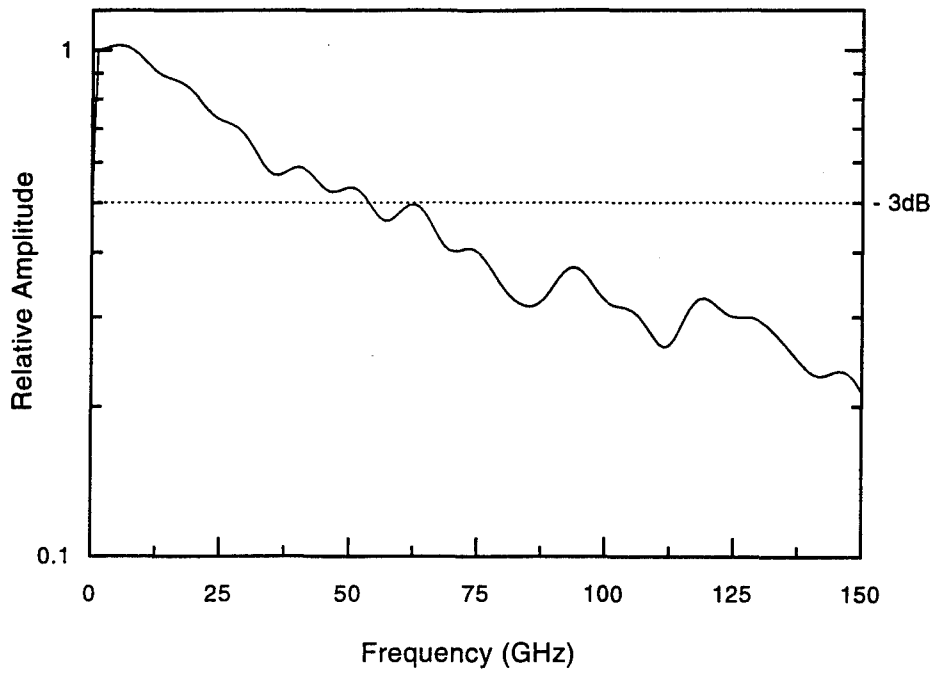


Fig. 17 Frequency response of LT-$In_{0.25}Ga_{0.75}As$ / $In_{0.25}Ga_{0.75}As$ photoconductor for an $In_{0.25}Ga_{0.75}As$ thickness of 1600 Å.

Figure 18 shows the dependence that the $In_{0.25}Ga_{0.75}As$ thickness has on both response time and responsivity. Plotted are the response times for $In_{0.25}Ga_{0.75}As$ thickness of 1600 Å, 2200 Å, and 2700 Å. We see that the response time slows with increased thickness. As the thickness increases so does the distance that deeply-generated carriers must move to reach the electrodes. Add to this the rapid reduction in the electric field strength, and we see how the response time can quickly erode. These deeply-generated carriers must be swept out before current stops flowing. The drift time for carriers generated 2200 Å below the surface can be several times longer than for carriers at the surface, up to 15 ps. Carriers formed below the $In_{0.25}Ga_{0.75}As$ and in the LT- $In_{0.25}Ga_{0.75}As$ layer also move under a weak field, but drift for only

a few picoseconds (approximately 0.5 μm) before being trapped. If they transfer into the stoichiometric regime they will contribute to the current until being collected. We see that changing the thickness of the InGaAs layer allows us to trade off speed for sensitivity. After accounting for Fresnel losses (32% reduction) and a 50% loss due to 50/50 electrode masking, the quantum efficiency for a responsivity of 0.15 A/W is 85%.

Figure 19 shows the sensitivity vs. wavelength curve for the heterostructure. In contrast to GaAs, the responsivity drops off gradually as we near the absorption edge (~1200 nm). The soft edge near 900 nm and the precipitous decline thereafter is probably the result of absorption in the graded region beneath the LT-$In_{0.25}Ga_{0.75}As$ layer. This layer has a linearly changing absorption edge that would account for the decline.

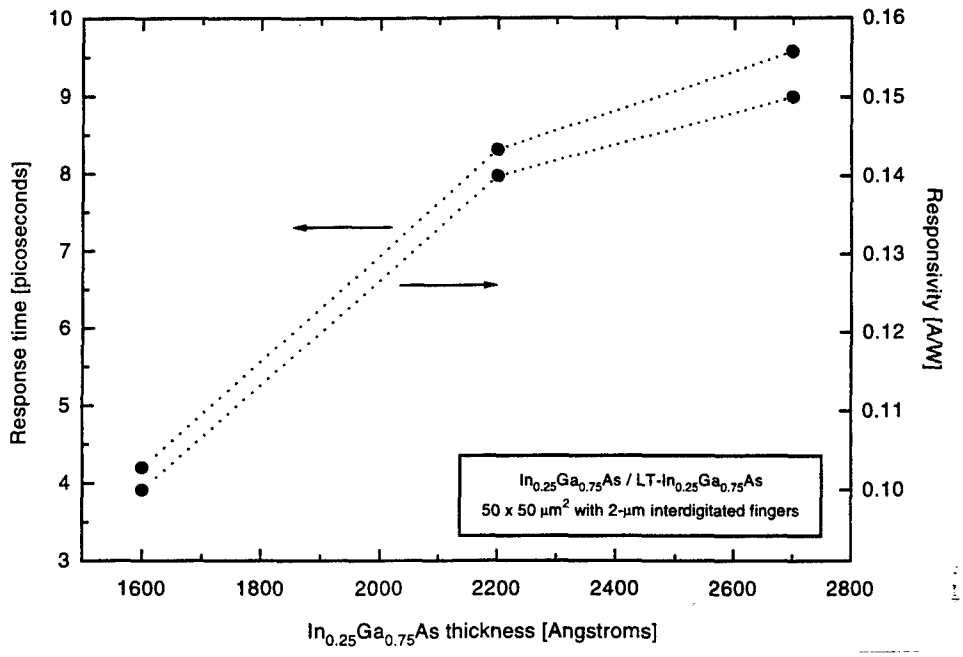


Fig. 18 Dependence of response time and sensitivity on the thickness of $In_{0.25}Ga_{0.75}As$ layer.

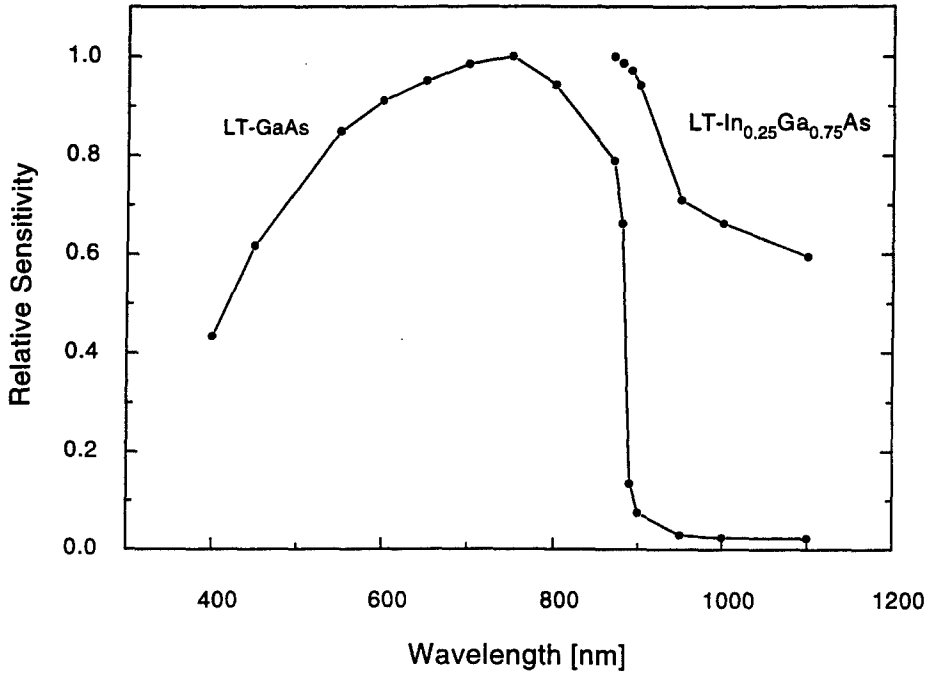


Fig. 19 Sensitivity of the LT-$In_{0.25}Ga_{0.75}As$ / $In_{0.25}Ga_{0.75}As$ photoconductor vs. wavelength.

E. Conclusion

This Phase I effort has been highly successful. The MSM photogate we developed has a demonstrated response time of 5 ps, making it the fastest sampling element currently available for application with high speed oscilloscopes. We demonstrated the use of a transimpedance amplifier with the gate to enhance sensitivity. With further modifications to the amplifier, we will be able to measure signals below 1 μV in amplitude. Also, we showed that the sampling gate works well with on-wafer probes for testing devices in wafer form. Finally, we began our investigation of low-temperature MBE-grown $In_{0.25}Ga_{0.75}As$. Preliminary results on this system are promising, although more work is needed to assure that low leakage current poses no problem. During the Phase II portion of this program we will concentrate on developing the sampling gate into a complete oscilloscope system. This will require us to develop LT-$In_{0.53}Ga_{0.47}As$ so that we can utilize compact, long-wavelength lasers as the driver for the photogate. We will also develop the synchronization electronics and software to provide a complete oscilloscope package to the end user.

F. References

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